WHAT IS CLAIMED IS:

1. A burn-in method comprising the steps of:

situating a burn-in frame on a flexible layer, the burn-in frame having at least one window and including resistors with resistor pads;

situating at least one integrated circuit chip having chip pads in the at least one window;

forming via openings in the flexible layer extending to the chip pads and the resistor pads;

applying a pattern of electrical conductors over the flexible layer and extending into the vias; and

burning in the at least one integrated circuit chip.

2. The method of claim 1, wherein the burn-in frame further includes fuses having fuse pads and the step of forming via openings includes forming via openings extending to the fuse pads.

3. The method of claim 2, wherein the burn-in frame further includes bias tracks and the step of forming via openings includes forming via openings extending to the bias tracks.

4. The method of claim 1, wherein the step of situating the burn-in frame occurs prior to the step of situating the at least one integrated circuit chip.

5. The method of claim 1, wherein the step of applying the pattern of electrical conductors includes applying a pattern of electrical conductors including test pads situated over the flexible layer.

6. The method of claim 5, further including the steps of after burning in the at least one integrated circuit chip, electrically isolating the chip pads and testing the at least one integrated circuit chip through the test pads.

7. A burn-in method comprising the steps of:

situating a burn-in frame on a flexible layer, the burn-in frame having at least one window and including resistors having resistor pads;

situating at least one multichip module having module pads in the at least one window;

forming via openings in the flexible layer extending to the module pads and the resistor pads;

applying a pattern of electrical conductors over the flexible layer and extending into the vias; and

burning in the at least one multichip module.

8. The burn-in method of claim 7, wherein the step of situating the at least one multichip module comprises situating a plurality of chips having chip pads and a common substrate in the at least one window and the module pads comprise chip pads, prior to coupling the chip pads;

wherein the step of applying pattern of electrical conductors over the flexible layer includes coupling the chip pads by applying a pattern of electrical conductors that couples selected chip pads of the plurality of chips.

9. The method of claim 7, wherein the step of applying the pattern of electrical conductors includes applying a pattern of electrical conductors including test pads situated over the flexible layer and further including the steps of after burning in the at least one multichip

module, electrically isolating the chip pads and testing the at least one integrated circuit chip through the test pads.

10. A burn-in and test method comprising the steps of:

situating a burn-in frame on a flexible layer, the burn-in frame having at least one window and including resistors having resistor pads, fuses having fuse pads, and voltage bias tracks;

situating at least one integrated circuit chip having chip pads in the at least one window and on the flexible layer;

forming via openings in the flexible layer extending to the chip pads, the resistor pads, the fuse pads, and the voltage bias tracks;

applying a pattern of electrical conductors over the flexible layer and extending into the vias, the pattern of electrical conductors including test pads situated over the flexible layer;

burning in the at least one integrated circuit chip;

electrically isolating the chip pads; and

testing the at least one integrated circuit chip through the test pads.

11. The method of claim 10, wherein the step of applying the pattern of electrical conductors includes positioning the test pads so as to reconfigure a chip pad layout, and

further including, after burning in and testing the at least one integrated circuit chip, applying a pattern of solder paste to the test pads and reflowing the solder paste into a solid solder contact.

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12. A burn-in fixture comprising:

burn-in frame having at least one window and including resistors having resistor pads;

at least one integrated circuit chip having chip pads and situated in the at least one window;

a flexible layer attached to the burn-in frame and the at least one integrated circuit chip, the flexible layer having via openings extending to the chip pads and the resistor pads;

a pattern of electrical conductors extending over the flexible layer and extending into the vias; and

means for burning in the at least one integrated circuit chip.

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~~13~~. The fixture of claim ~~12~~, wherein the burn-in frame further includes fuses having fuse pads and voltage bias tracks, and wherein the via openings extend to the fuse pads and voltage bias tracks.

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